MEMORY DEVICE, REFRESH CONTROL CIRCUIT TO BE USED FOR THE MEMORY DEVICE, AND REFRESH METHOD

CROSS REFERENCES TO RELATED APPLICATIONS

5   [0001]

The present document is based on Japanese Priority Document JP 2003-062774, filed in the Japanese Patent Office on March 10, 2003, the entire contents of which being incorporated herein by reference.

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BACKGROUND OF THE INVENTION

[0002]

1. Field of the Invention

[0003]

15   The present invention relates to a memory device of a dynamic type such as a dynamic random access memory (DRAM), a refresh control circuit to be used for the memory device, and a refresh method.

[0004]

20   2. Description of the Related Art

[0005]

A memory device of a dynamic type has been conventionally used as a memory device applicable to a computer apparatus and the like. As a typical memory

25   device, a semiconductor memory device such as the so-called DRAM is known.

[0006]

FIG. 9 shows an example of the schematic configuration of a memory cell 900. The memory cell 900

30   uses a transistor element 901 as a switching element. The turning on and off of the transistor element 901 is

controlled through a word line 903. Data (charge)
writing and data reading of the memory cell 900 are set
to be controlled through a bit line 902. The charge
quantity held in a capacitor (an electric capacity unit)
904 of the memory cell 900 is gradually decreased at
every performance of a read operation, or owing to
various kinds of parasitic capacitance and natural
discharge. When the charge quantity becomes smaller than
a fixed value, the content stored in the capacitor 904 is
lost (or volatilized). Accordingly, such a memory device
of a dynamic type as the DRAM needs the so-called refresh
operation, by which charge held in the memory cell 900
till then is amplified and is re-written.
[0007]

A typical example of this kind of dynamic-type
memory device, a DRAM 800, as schematically simplified to
be shown in FIG. 10, includes a memory array unit 801 and
a memory control unit 820 as its principal parts. The
memory array unit 801 is structured to arrange memory
elements (memory cells) 802 of a dynamic type in an array.
The memory elements 802 severally store information in
the state of binary numbers based on a charge holding
state and a charge not holding state. The memory control
unit 820 is provided between the memory array unit 801
and an external memory control device 810. The memory
control unit 820 controls the reading of information from
the memory array unit 801 and the writing of information
to the memory array unit 801 in accordance with a command
signal and the like from the memory control device 810.
[0008]

This kind of the memory device (the DRAM 800) has an

auto-refresh function for performing a refresh operation on the basis of a refresh request from the external memory control device 810, and a self refresh function for executing a refresh operation automatically at every satisfaction of a set condition, such as every elapse of a predetermined time, every decrease of a held charge quantity under a predetermined value, or the like, after the condition of the memory device has been set by the external memory control device 810.

[0009]

A refresh operation of a memory device of a dynamic type like a DRAM in a case of the self refresh function is once performed at every elapse of the time of tREF/m, where "tREF" designates a memory holding time and "m" designates the number of addresses necessary for refreshing the whole memory addresses. For example, supposing that tREF = 64[ms] and m = 4096, the refresh operation is performed at every elapse of 15.6 [μs].

[0010]

In many cases, such a self refresh function is generally adopted as a refresh method in a DRAM or the like to be used for electric equipment, such as a personal computer or a mobile telephone, which uses a small-sized battery having a limited capacity as its power source and is needed to hold stored contents for a long time.

[0011]

Now, because the above-mentioned self refresh function performs amplification of the charges held in the memory cells and the re-writing of the amplified charges to the original memory cells, the performance of

the self refresh function needs electric power at the
time of the amplification. Consequently, the performance
consumes electric power therefor from a power system.
Because it is requested for electric equipment such as a
5   personal computer and a mobile telephone to be used
without additional charging of a power source such as a
battery having a limited capacity for a long time, the
self refresh function performed in a DRAM or the like is
strongly requested to decrease power consumption at the
10   time of the performance of the function.
[0012]

     Accordingly, in a conventional technique, a method
has been proposed. By the method, a mode register 821 is
provided in the memory control unit 820 for decreasing
15   the current consumption at the self refresh function, and
the self refresh function is performed only to a
predetermined memory space in conformity with a control
condition set in the mode register 821.
[0013]

20   For example, Patent Document 1 proposes an invention
by which whether each of the addresses is a using memory
space or not is previously stored to all of the addresses
of a memory cell array, and refreshing is not performed
to the addresses which are not used (not a using memory
25   space). A further concrete aspect thereof is a method by
which boundary addresses between a using memory space and
a not using memory space in the whole address space are
previously stored, and the refreshing is not performed to
the not using memory space having the addresses larger
30   than the boundary addresses. However, the conventional
invention does not aim the decrease of power consumption

as a first primary object, rather aims to prevent the
lowering of a processing data rate. Consequently, the
technique of this Patent No. 2829998 cannot always
achieve the decrease of power consumption.

5   [0014]

Alternatively, as another conventional technique for
controlling such kind of refresh function, for example, a
technique schematically shown in FIGS. 11 and 12 is known.
That is, correspondence relations between the contents of
10   the setting of the control method of the mode register
821 storing two-bit information and the memory spaces to
which self refreshing is performed are determined in
advance. In addition, all of the address spaces are
previously divided into a plurality of memory spaces such
15   as a memory space A, a memory space B, a memory space C
and a memory space D, and the contents of the mode
register 821 is made to be written at the time of the
starting of the memory device. Then, for example, in a
case where the contents of the mode register 821 is "11",
20   self refreshing is performed only to the memory space A,
a top quarter of the whole memory space of the memory
device, and the self refreshing is not performed to the
other part of the whole memory space (i.e., the self
refreshing at that time is omitted). In such a way, as
25   shown in FIG. 12, only the quarter of the whole address
space receives the self refresh operation, the current
consumption necessary for the self refresh operation at
that time can be decreased to about a quarter of the
current consumption necessary for the self refresh
30   operation for the whole address space.

[0015]

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Alternatively, for example, Patent Document 2 proposes a technique for realizing an inexpensive memory having a large memory capacity and a small data holding current by modularizing a DRAM, a static random access memory (SRAM) and a nonvolatile memory device into a package.

[0016]

[Patent Document 1]: Japanese Patent No. 2829998 (Claims and the Whole Detailed Description of the Invention)

[0017]

[Patent Document 2]: Japanese Patent Application Laid-Open Publication No. 2001-344967 (Claims and the Whole Detailed Description of the Invention)

[0018]

However, because the technique proposed by the Patent Document 1 stores whether each address of the whole address of the memory cell array is a using memory space or not, the technique has a problem such that memory means for the storage and means for reading data from the memory means and for discriminating the necessity of refreshment of all of the addresses to control the refreshment operation become very complicated. In addition, because the memory cell array has a tendency to increase its capacity more and more, the number of addresses further increases. Consequently, there is another problem such that the means for storing whether all of the addresses are severally using memory spaces or not to discriminate the addresses is obliged to be complicated more and more.

[0019]

Moreover, as a further detailed aspect, boundary

addresses of using memory spaces and not using memory spaces in the whole address space are previously stored, and refreshment is not performed to not using memory spaces having larger addresses than the boundary

5   addresses. However, by such a method, refreshment is performed to the spaces before the boundary addresses and is not performed to the spaces after the boundary addresses. In such a way, the whole address space can be divided into only two spaces at the boundary addresses as

10   a boundary line. Consequently, for example, the following control cannot be realized: the whole address space is divided into four memory spaces, and only the second memory space and the third memory space of the four spaces from the top are in use and refreshment is

15   performed to the second and the third memory spaces.
[0020]

Moreover, in the refresh method schematically shown in FIGS. 11 and 12, which may be a variation of such a technique of the invention proposed in the Patent

20   Document 1, the setting of the mode register 821 is performed at the time of turning of its power source or at the time of initialization such as system resetting. Consequently, the refreshing method is effective to a case where the memory space to be stored and held

25   minimally is previously known like a case such as an operating system (OS), but the refreshing method has a problem in which memory spaces cannot be utilized effectively sometimes or the decrease of power consumption cannot be achieved effectively sometimes in a

30   case where the spaces actually necessary to be used vary dependently on the sizes of data to be stored each time

such as a user space, because the memory spaces to be actually used become different from the setting at the time of turning on its power source or at the time of initialization such as system resetting.

[0021]

For example, in a case where refreshment is set to be performed only to the memory space A at the time of initialization, when the quantity of data to be stored becomes large and all of the memory space A is used, and also when the memory space B is tried to be used in such a case, it is set not to perform refreshment to the memory space B, and consequently the memory space B cannot be used in effect.

[0022]

Furthermore, by the technique according to the invention proposed by the Patent Document 1, in a case where the memory spaces A, C and D are not in use and only the memory space B is in use, the boundary addresses are located at the end of the memory space B, and consequently refreshment is performed also to the memory space A, which is not to be needed to be refreshed actually, in vain. Hence, sufficiently effective decrease of power consumption cannot be achieved by the technique. This situation also applies to the technique shown in FIGS. 11 and 12.

[0023]

Moreover, the technique proposed by the Patent Document 2 modularizes a DRAM device, an SRAM device, a nonvolatile memory device into a package, but does not perform the decrease of power consumption of each device. Consequently, it is needless to say that the technique

cannot achieve the decrease of power consumption of the memory device of a dynamic type such as the DRAM device. Moreover, because the DRAM device, the SRAM device and the nonvolatile memory device are modularized in one package, there is possibility that the whole configuration thereof becomes very complicated.

SUMMARY OF THE INVENTION

[0024]

The present invention was made in consideration of such problems, and aims to provide a simply configured memory device which can achieve a sufficiently effective decrease of the consumption power of a refresh operation of the memory device even if the sizes of memory spaces to be used change each time, a refresh control circuit to be used for the memory device, and a refresh method.

[0025]

A first memory device according to an aspect of the present invention is a semiconductor memory device of a dynamic type for refreshing information stored in a memory space to hold the information continuously by amplifying the information stored in the memory space to rewrite the amplified information in the memory space. The semiconductor memory device includes a refresh control circuit for performing refreshment of the information only to a sub memory space which is in use when the refreshment of the information is performed, the sub memory space holding the information necessary to be refreshed, among a plurality of sub memory spaces formed by previous division of the memory space.

[0026]

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A second memory device according to an aspect of the present invention is a semiconductor memory device of a dynamic type including a memory cell array. The memory device has the memory cell array for storing information, and a refresh circuit for refreshing the information stored in the memory cell array to hold the information continuously by amplifying the information stored in the memory cell array to rewrite the amplified information in the memory cell array. The memory device includes a refresh control circuit for controlling an operation of the refresh circuit so as to perform refreshment of the information only to a sub memory space which is in use when the refreshment of the information is performed, the sub memory space holding the information necessary to be refreshed, among a plurality of sub memory spaces formed by previous division of an address space in a memory space of the memory cell array.

[0027]

A first refresh control circuit according to an aspect of the present invention is a refresh control circuit to be used for the first memory device described above.

[0028]

A second refresh control circuit according to an aspect of the present invention is a refresh control circuit to be used for the second memory device described above.

[0029]

A first refresh control method according to an aspect of the present invention is a method for refreshing storage in a memory device of a dynamic type

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for refreshing information stored in a memory space to hold the information continuously by amplifying the information stored in the memory space to rewrite the amplified information in the memory space. The method includes the steps of: dividing the memory space into a plurality of sub memory spaces in advance; and performing refreshment of the information only to a sub memory space among the plurality of sub memory spaces, the sub memory space being in use when the refreshment of the information is performed, the sub memory space holding the information necessary to be refreshed.

[0030]

A second refresh control method according to an aspect of the present invention is a refresh method for refreshing information stored in a memory cell array to hold the information continuously by amplifying the information to rewrite the amplified information in the memory cell, the memory cell array is provided in a memory device of a dynamic type. The method includes the steps of: dividing an address space in a memory space of the memory cell array into a plurality of sub memory spaces in advance; and performing refreshment of the information only to a sub memory space among the plurality of sub memory spaces, the sub memory space being in use when the refreshment of the information is performed, the sub memory space holding the information necessary to be refreshed.

[0031]

In the first memory device, the first refresh control circuit or the first refresh control method according to the aspects of the present invention, a

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memory space is previously divided into a plurality of sub memory spaces. Moreover, the refreshment of information is performed only to a sub memory space which is in use at the time of the refreshment of the

5   information and holds the information necessary to be refreshed among the plurality of sub memory spaces. The refreshment of the information is not performed to the sub memory spaces which are not in use at the time of the refreshment and do not need the refreshment.

10   Consequently, the refreshment to such parts unnecessary to be refreshed is omitted, and thereby at least the decrease of the power consumption required for refreshing that parts can be achieved.

[0032]

15   In the second memory device, the second refresh control circuit or the second refresh control method according to the aspects of the present invention, an address space in a memory space of a memory cell array is previously divided into a plurality of sub memory spaces.

20   Moreover, the refreshment of information is performed to a sub memory space which is in use at the time of the refreshment of the information and holds the information necessary to be refreshed among the plurality of sub memory spaces. The refreshment of the information is not

25   performed to the sub memory spaces which are not in use at the time of the refreshment and do not need the refreshment. Consequently, the refreshment to such parts unnecessary to be refreshed is omitted, and thereby at least the decrease of the power consumption required for

30   refreshing that parts can be achieved.

[0033]

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Hereupon, the first memory device, the first refresh control circuit or the first the refresh control method according to the aspects of the present invention can be applied to a memory device of a dynamic type, a refresh

5   control circuit or a refresh control method which stores information into a memory space, and which amplifies the information stored in the memory space to rewrite the amplified information into the memory space , and further which refreshes the information to hold continuously

10   thereby. Consequently, it is needless to say that the memory device to which the present invention can be applied is not always limited only to the memory device, such as a DRAM, which stores information as binary data based on a charge holding state and a not charge holding

15   state in a memory cell. However, more specifically, the present invention is suitably applied to a semiconductor memory device, such as a DRAM, among existing kinds of memory devices. Such a semiconductor memory device of a dynamic type includes a memory cell array for storing

20   information, and a refresh circuit for refreshing the information stored in the memory cell array to hold the information continuously by amplifying the information and re-writing the information into the memory cell array. That is, the second memory device, the second refresh

25   control circuit or the second refresh control method according to the aspects of the present invention is suitable for the memory device of a dynamic type provided with such a memory cell array.

[0034]

30   Incidentally, the refresh control circuit may operates a logical product of data pertaining to whether

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each of the sub memory spaces is in use or not and refresh address data to be input to each address, and may perform control of whether the refreshment is performed or not to each sub memory with the refresh circuit on the

5   basis of a result of the operation. The reason of adopting such a configuration is that the configuration of the principal part of the refresh control circuit preferably becomes simple.

[0035]

10   Moreover, a row decoder may be added to the memory cell array, and the row decoder may be set to specify a row address to which the refreshment is performed in addresses of the memory cell array, and further a refresh control circuit may be inserted between the memory cell

15   array and the row decoder to intervene in a function of the row decoder for specifying the row address to which the refreshment is performed for controlling whether the refreshment is performed or not to each of the sub memory spaces. Alternatively, the refresh control circuit may

20   be provided (built) in the row decoder.

[0036]

In such a configuration, it preferably becomes possible to add the refresh control circuit easily to a memory device having an existing general circuit

25   configuration without complicating the circuit system thereof.

[0037]

Alternatively, a row decoder and a refresh address counter may be added to the memory cell array, and the

30   row decoder and the refresh address counter may be set to specify the row address to which the refreshment is

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performed in addresses of the memory cell array, and
further a refresh control circuit may be attached to the
refresh address counter to intervene in a function of the
refresh address counter for outputting the row address to

5   which the refreshment is performed for controlling
whether the refreshment is performed or not to each of
the sub memory spaces. Alternatively, the refresh
control circuit may be provided in the refreshment
address counter.

10   [0038]

In such a configuration, it preferably becomes
possible to add the refresh control circuit easily to a
memory device having an existing general circuit
configuration without complicating the circuit system

15   thereof.

[0039]

Alternatively, a row decoder, a multiplexer and a
refresh address counter may be connected to the memory
cell array in this order, and the row decoder, the

20   multiplexer and the refresh address counter may be set to
specify the row address to which the refreshment is
performed in addresses of the memory cell array, and
further a refresh control circuit may be inserted between
the refresh address counter and the multiplexer to

25   intervene in a refresh address counter's output of the
row address to which the refreshment is performed, the
output transmitted to the row decoder through the
multiplexer, for controlling whether the refreshment is
performed or not to each of the sub memory spaces.

30   Alternatively, the refresh control circuit may be
provided in the multiplexer.

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[0040]

In such a configuration, it preferably becomes possible to add the refresh control circuit easily to a memory device having an existing general circuit configuration without complicating the circuit system thereof.

[0041]

Moreover, in a case where the memory space is previously divided into different memory spaces to store different kinds of contents of information from one another, at least one of the divided memory spaces may be further divided into the plurality of sub memory spaces.

[0042]

Such a configuration makes it possible to subdivide a memory space divided (assigned) as, for example, a user space into a plurality of sub memory spaces to discriminate whether to perform refreshment or whether to omit the refreshment to each of the sub memory spaces on the basis of whether the memory spaces are in use at the time of refreshment or not, namely whether refreshment is actually necessary or not. In addition, the refreshment is not performed to the memory spaces unnecessary to be refreshed, and the refreshment is performed to the memory spaces necessary to be refreshed. Thereby, all of the memory spaces are always made to be usable for the storage of information, and power consumption owing to unnecessary refreshment can be decreased.

BRIEF DESCRIPTION OF THE DRAWINGS

[0043]

The above and other objects, features and advantages

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of the present invention will become more apparent from the following description of the presently preferred exemplary embodiments of the invention taken in conjunction with the accompanying drawings, in which:

[0044]

FIG. 1 is a diagram showing a schematic configuration of a memory device according to an embodiment of the present invention;

[0045]

FIG. 2 is a diagram showing a configuration of a principal part of a refresh control circuit;

[0046]

FIG. 3 is a table showing relations between contents of information held in each bit in a using memory space register and a region to be an object to which self refreshment is performed;

[0047]

FIG. 4 is a block diagram showing a schematic configuration of a DRAM being the memory device according to a first embodiment;

[0048]

FIG. 5 is a block diagram showing a principal part of a refresh control circuit extracted from the DRAM being the memory device according to the first embodiment;

[0049]

FIG. 6 is a block diagram showing one of variations of the principal part of the refresh control circuit in the DRAM being the memory device according to the first embodiment;

[0050]

FIG. 7 is a block diagram showing a schematic configuration of a DRAM being a memory device according to a second embodiment;

[0051]

FIG. 8 is a block diagram showing a schematic configuration of a DRAM being a memory device according to a third embodiment;

[0052]

FIG. 9 is a circuit diagram showing an example of a schematic configuration of a memory cell in a conventional general DRAM;

[0053]

FIG. 10 is a block diagram showing a schematic configuration of the conventional general DRAM;

[0054]

FIG. 11 is a table showing relations between contents of information held in a mode register of a memory device based on a conventional technique and spaces to be a target to which self refreshment is performed; and

[0055]

FIG. 12 is a timing chart pertaining to a self refresh operation in the memory device based on the conventional technique.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0056]

In the following, the preferred embodiments of the present invention will be described in detail by reference to the attached drawings.

[0057]

FIG. 1 is a diagram showing a schematic configuration of a memory device according to an embodiment of the present invention by simplifying the memory device. Incidentally, because a refresh method

5   according to the present invention is embodied by an operation or work of the memory device, and because a refresh control circuit according to the present invention is used by being incorporated in the memory device, the refresh method and the refresh control

10   circuit will be described in the following together with the memory device.

[0058]

The principal part of the memory device includes a memory cell array 11, a refresh circuit 20, a refresh

15   control circuit 30 and a data read/write circuit 40. The memory device is a dynamic-type one such as a DRAM. Incidentally, the refresh circuit 20, the refresh control circuit 30 and the data read/write circuit 40 can be collectively called as a memory control unit 50.

20   [0059]

The memory cell array 11 is made by arranging memory cells having a schematic configuration exemplified in FIG. 9 schematically in an array. The memory cell array 11 stores data (information) transmitted from an external

25   memory control device 60. Because charges held in the memory cell array 11 naturally decrease or are extracted to the outside at the time of reading of data, it is needed to refresh the memory cell array 11 at every predetermined timing, or to refresh it when the charge

30   held by several memory cell becomes less than a predetermined level. The memory cell array 11 is similar

to the one used in a conventional general memory device
of a dynamic type such as a DRAM.
[0060]

The data read/write circuit 40 has a function of
5   writing the data transmitted from the external memory
control device 60 on the outside of the memory device
into a corresponding address in the memory cell array 11
and a function of reading the data stored in the memory
cell array 11 on the basis of the data, and a command
10   signal for the writing or the reading. The data writing
function and the data reading function of the data
read/write circuit 40 to and from the memory cell array
11 are also basically similar to the ones used for the
conventional general memory device of a dynamic type such
15   as the DRAM.
[0061]

The refresh circuit 20 basically has a function of
amplifying the data stored in the memory cell array 11 at,
for example, every predetermined timing such as a fixed
20   refresh period to rewrite the amplified data in the
memory cell array 11, and thereby of refreshing the data
to hold the data continuously. Incidentally, the refresh
circuit 20 is set so that the operation of the refresh
circuit 20 is controlled by the refresh control circuit
25   30, which will be described later, so as not to perform
the refreshment of the memory cells in the memory spaces
which are not used at the time of the performance of
refresh operation and are substantially unnecessary for
being refreshed. The refresh circuit 20 may be set to
30   perform the above-mentioned refreshment of data through
the data read/write circuit 40, or may be set to perform

the above-mentioned refreshment of data directly to the memory cell array 11 through another route from the data read/write circuit 40. However, it is needless to say that it is more general to perform the data refreshment through the data read/write circuit 40 or in cooperation with the data read/write circuit 40.

[0062]

The refresh control circuit 30 performs the control such that the address space in the memory space of the memory cell array 11 is previously divided (allotted) into a plurality of sub memory spaces, and that the data refreshment is performed only to the sub memory spaces which have been used immediately before the refreshment and includes memory cells holding data (charges) necessary to be refreshed among the plurality of the sub memory spaces, but that the data refreshment is not performed to the memory spaces which have not been in use and includes no memory cells holding data (charges) at all not to need the refreshment.

[0063]

The principal part of the refresh control circuit 30 can be configured to be the one exemplified in FIG. 2 more in detail. The refresh control circuit 30 includes a using memory space register 31 and a plurality of AND circuit elements 32a, 32b, 32c and 32d, the number of which corresponds to the plurality of sub memory spaces. Incidentally, hereupon for simplifying the description and illustration, the refresh control circuit 30 will be described on an assumption that the whole memory space of the memory cell array 11 is divided into four sub memory spaces of A, B, C and D.

[0064]

     The using memory space register 31 stores four-bit memory using memory space information of A, B, C and D corresponding to the sub memory spaces A, B, C and D,

5   respectively. The memory using memory space information can be obtained from the write data, their address data, command signals for writing commands or reading commands, and the like, all transmitted from the external memory control device 60 to the memory device 30.

10   [0065]

     More specifically, for example, when even one address in the sub memory space A is in use at the time of writing or reading immediately before a refresh operation, the memory using space information pertaining

15   to the sub memory space A takes "1" as the information indicating "in use", and the information "1" is stored (memorized) in the bit A of the using memory space register 31. Alternatively, when all of the addresses in the sub memory space A are not in use at the time of

20   writing or reading immediately before refresh operation, the memory using space information pertaining to the sub memory space A takes "0" as the information indicating "not in use", and the information "0" is stored in the bit A of the using memory space register 31.

25   [0066]

     A plurality (herein four) of AND circuit elements 32a, 32b, 32c and 32d severally take a logical product of a self refresh starting signal and an output of the using memory space register 31 to output or not to output self

30   refresh operation signals A', B', C' and D', respectively. The self refresh starting signals are signals for

specifying the addresses to be the objects of self
refreshment. The self refresh starting signals are
output from, for example, a self refresh timer or a
refresh address counter, which are not shown in FIG. 1.
5   The self refresh starting signals outputs, for example,
"1" in the order A', B', C', D', A', B', C', D' … .
[0067]

     These AND circuit elements 32a, 32b, 32c and 32d
operate logical products of the data ("1" or "0") of the
10   memory using space information stored in the using memory
space register 31 and the self refresh starting signals
("1") input at predetermined timing in order (for example,
periodically). When an operation result is "1", or in a
case where the data of the memory using space information
15   is "1" indicating the sub memory space being in use when
the self refresh starting signal "1", the operation
result becomes 1 × 1 = 1, and the result is output as the
self refresh operating signal. However, in a case where
the data of the memory using space information is "0"
20   indicating the sub memory space being not in use when the
self refresh starting signal "1" is input, the operation
result becomes 1 × 0 = 0. Consequently, the self refresh
operating signal is not output in this case. That is, as
schematically shown in FIG. 3 as a list, when the data of
25   the memory using space information is that bit A = 1, the
sub memory space A is an object of the self refreshment.
When the data of the memory using space information is
that bit B = 1, the sub memory space B is an object of
the self refreshment. When the data of the memory using
30   space information is that bit C = 1, the sub memory space
C is an object of the self refreshment. When the data of

the memory using space information is that bit D = 1, the sub memory space D is an object of the self refreshment, and so forth. As above, whether self refreshment of the four sub memory spaces A, B, C and D is performed or not is severally controlled independently according to whether they are in use or not until immediately before the self refreshment.

[0068]

More specifically, for example, in a case where only the sub memory space B is in use and the other sub memory spaces A, C and D are not in use until immediately before self refreshment is exemplified, only the logical product at the bit of the sub memory space B becomes $1 \times 1 = 1$, and only the self refresh operation signal B' is output because the data stored in the using memory space register 31 are A = 0, B = 1, C = 0 and D = 0 in this case. Then, the refresh circuit 20 receives the self refresh operating signal B', and performs self refreshment only to the sub memory space B. The refresh circuit 20 does not perform the self refreshment to the other sub memory spaces A, C and D (the refreshment is daringly omitted).

[0069]

In such a way, it becomes possible that self refreshment is performed to the sub memory spaces to which storage holding is necessary, and that self refreshment is not performed to the sub memory spaces which have not to be used, and to which storage holding is not necessary. As a result, it becomes possible to achieve decreasing the power consumption owing to unnecessary self refreshment greatly.

[0070]

[First Embodiment]

[0071]

FIG. 4 shows the schematic configuration of a memory
device (DRAM) according to a first embodiment. The DRAM
includes the following components as its principal part:
a clock buffer 1, a command decoder 2, a timing generator
3, a temperature detection means 4, a self refresh timer
5, a refresh address counter 6, a row address latch 7, a
column address latch 8, a multiplexer 9, a row decoder 10,
a memory cell array 11, a sense amplifier 12, a column
decoder 13, a data input/output buffer 14 and a refresh
control circuit 30. Hereupon, the self refresh timer 5,
the refresh address counter 6, the row address latch 7,
the column address latch 8, the multiplexer 9, the row
decoder 10, the sense amplifier 12 and the column decoder
13 collectively correspond to the refresh circuit 20
described in the former embodiment substantially.
Moreover, the row address latch 7, the column address
latch 8, the multiplexer 9, the row decoder 10, the sense
amplifier 12 and the column decoder 13 correctively
correspond to the data read/write circuit 40 described in
the former embodiment substantially.

[0072]

The clock buffer 1 receives a clock signal from the
outside to distribute the received clock signal to the
internal circuits. The command decoder 2 decodes a
command signal from the outside to discriminate the
operation such as writing, reading or automatic
refreshing. The timing generator 3 generates various
kinds of timing necessary for internal operation. The

temperature detection means 4 detects a temperature in the DRAM, a temperature in the vicinity of the memory cell array 11 or the like.

[0073]

The self refresh timer 5 generates a clock for determining an operation interval at the time of a self refreshing mode. The refresh address counter 6 counts up its counted value one by one every performance of refreshment operation at the time of automatic refreshment from the outside and self refreshment, and outputs row addresses at the time of refreshment in order.

[0074]

The row address latch 7 and the column address latch 8 separates the address signal transmitted from the outside in time division into row addresses and column addresses to store the addresses temporarily.

[0075]

The multiplexer 9 selects either refreshment addresses or row addresses at the time of ordinary operation (at the time of the operation of writing or reading) on the basis of the command signal at that time, or the like. The row decoder 10 selects one row (one line) among all of the m row arrays (m row lines) at a time.

[0076]

The memory cell array 11 comprises memory cells arranged in an orthogonal array made of m rows $\times$ n columns. Each memory cell stores information in a binary state of holding charges or not holding charges. When one row is selected, the charges held by each of the n memory cells connected the selected row as information

are read out (are extracted) to the sense amplifier 12.
At this time, it is needless to say that it is regarded
that the information "0" can be read from a memory cell
holding substantially no charge.

[0077]

     The sense amplifier 12 amplifies the charges read
from the memory cells as information at a predetermined
gain to convert the charges to a data signal, and outputs
the data signal. The column decoder 13 selects a column
corresponding to a data signal from the outside among the
n columns (n pieces) on the basis of the data signal and
an address signal from the outside.

[0078]

     The data input/output buffer 14 functions as a
buffer for inputting the data to be written into the
sense amplifier 12 at the time of a writing operation,
and functions as a buffer for outputting the data read at
the time of a reading operation to the outside.

[0079]

     In reading operation of the so-called general DRAM
configuration which has been described above and does not
include the refresh control circuit 30, a row line is
selected on the basis of the row address specified by an
external address signal. Then, the data (the information
held as the existence or the nonexistence of charges)
held in the memory cells of each of the n columns
connected to the selected row line is read to be
amplified by the sense amplifier 12. Then, the data of
each column amplified by the sense amplifier 12 is
collected to be a data signal (read data) of a group
composed of the amplified data of a column at every

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column by the column decoder 13, and the data signal is selected by the sense amplifier 12. The selected data signal is output to the outside through the data input/output buffer 14.

5 [0080]

Moreover, in a writing operation, the data stored in the memory cell array 11 is read at every row, and is amplified by the sense amplifier 12. After that, the information held by each of the memory cells connected to

10 the column specified by the column decoder 13 is replaced with the write data from the outside, thereby writing (re-writing) is performed.

[0081]

The refresh control circuit 30 is inserted between

15 the row decoder 10 and the memory cell array 11. When refresh operation is performed, the refresh control circuit 30 performs the following control. That is, the address space in the memory space of the memory cell array 11 is previously divided into a plurality of sub

20 memory spaces. The sub memory spaces are allotted so that refreshment control can be performed to each of them separately. Data refreshment is performed only to the sub memory spaces having the memory cells which are in use immediately before the refreshment and hold the data

25 necessary to be refreshed among the plurality of sub memory spaces. The refreshment at that time is not performed to the memory spaces which are not in use and have no memory cells holding data at all not to need refreshment as a result. On the other hand, at the time

30 of an ordinary operation such as reading data or writing data, the refresh control circuit 30 does not intervene

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in the function of the row decoder 10 to the memory cell
array 11 so as not to disturb the ordinary row selection
function (for example, the operation of selecting rows
one by one line sequentially, or the like) as the row
5   decoder 10 at that time.
[0082]

     FIG. 5 shows the principal part of the refresh
control circuit 30 in the DRAM of the first embodiment by
extracting the principal part from the refresh control
10   circuit 30.   Incidentally, in FIG. 5, for simplifying
illustration and the description thereof, it is supposed
that each sub memory space includes five row lines
severally, and only the sub memory space A will be
extracted to be described among the sub memory spaces A,
15   B, C and D.   It is needless to say that the number of the
actual row lines (the number of rows) is far larger.
[0083]

     The refresh control circuit 30 of the first
embodiment includes the main body of the refresh control
20   circuit 30 and a refresh selection unit 33.   The main
body of the refresh control circuit 30 is configured as
illustrated in FIG. 2 to include the using memory space
register 31 and the AND circuits elements 32a, 32b, 32c
and 32d.   The refresh selection unit 33 receives the
25   output from the main body of the refresh control circuit
30.   Then, the refresh selection unit 33 performs either
of the following two operations.   That is, the refresh
selection unit 33 selects a row in the sub memory space A
for performing the refreshment of the sub memory space A
30   at the time of refreshment.   Alternatively, although the
row decoder 10 specifies the selection of a row in the

sub memory space A, the refresh selection unit 33
intervenes in the selection of the row decoder 10 at that
time to the sub memory space A so as not to select (omit)
the row in the sub memory space A.

5 [0084]

In the operation of the refresh control circuit 30,
for example, in the case where the sub memory space A is
in its using state and the output from the main body of
the refresh control circuit 30 is that the sub memory

10 space A = "1", the signal "1" is severally input into one
side terminals of AND circuits 34a, 34b, 34c and 34d of
the rows in the refresh selection unit 33. When a signal
"1" for specifying the selection of each row is line
sequentially input to the other side terminals of the AND

15 circuits 34a, 34b, 34c and 34d to each row from the row
decoder 10 as an ordinary self refreshment mode, the
logical products of the AND circuit 34a, 34b, 34c and 34d
become 1 × 1 = 1 in order. Consequently, ordinary self
refreshment is performed.

20 [0085]

However, in a case where the sub memory space A is
not in use and the output from the main body of the
refresh control circuit 30 is that the sub memory space A
= "0", the signal "0" is input into one side terminal of

25 the AND circuits 34a, 34b, 34c and 34d of the rows in the
refresh selection unit 33. Then, when a signal "1" for
specifying the selection is line sequentially input into
the other terminal of the AND circuits 34a, 34b, 34c and
34d of the rows from the row decoder 10 as the ordinary

30 self refreshment mode, the logical products of the AND
circuits 34a, 34b, 34c and 34d become 1 × 0 = 0 in order.

30

Consequently, the self refreshment is not performed in the sub memory space A.

[0086]

Moreover, at the time of an ordinary read operation or an ordinary write operation, the main body of the refresh control circuit 30 outputs the signal "1" to all of the sub memory spaces A, B, C and D, and thereby it is possible not to intervene the selection of the row decoder 10 to the memory cell array 11.

[0087]

Incidentally, the main body of the refresh control circuit 30 and the refresh selection unit 33 may be provided in the inside of the row decoder 10. Alternatively, as exemplified in FIG. 6, each refresh selection unit 33 of each sub memory space may be provided with a part of the refresh control circuit 30 for performing the control of the sub memory space therein (for example, the part for the sub memory space A (A bit) of the using memory space register 31 in the refresh control circuit 30 and the AND circuit 32a are provided in the refresh selection unit 33 for the sub memory space A).

[0088]

[Second Embodiment]

[0089]

FIG. 7 shows a schematic configuration of a memory device (DRAM) according to a second embodiment. In the second embodiment, an example of the configuration in which a refresh control circuit 30 is attached to a refresh address counter 6 will be described. Incidentally, the same reference numerals as those in the

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first embodiment are attached to the similar components as those in the first embodiment, and they will be referred to as the same names as those in the first embodiment. Furthermore, their detailed descriptions are omitted for simplifying the descriptions.

[0090]

The refresh control circuit 30 of the second embodiment performs the control of whether refreshment to each sub memory space is performed or not by intervening in the function of the refresh address counter 6 for outputting a row address to which refreshment is performed.

[0091]

In further detail, the refresh control circuit 30 as shown in FIG. 2 is attached to the refresh address counter 6. Assuming that a sub memory space A and a sub memory space C are in use at the time of refreshment, and that a sub memory space B and a sub memory space D are not in use, the refresh control circuit 30 intervenes in the output function of the refresh address counter 6 to input a signal "1" into the refresh address counter 6 as a self refreshment operation signal A' to the sub memory space A and a self refreshment operation signal C' to the sub memory space C, and to input a signal "0" into the refresh address counter 6 as a self refreshment operation signal B' to the sub memory space B and a self refreshment operation signal D' to the sub memory space D.

[0092]

The refresh address counter 6 is set so that, in response to the inputs, the refresh address counter 6 outputs the row addresses in the sub memory space A and

the sub memory space C correspondingly to the signal "1", and that the refresh address counter 6 does not output the row addresses in the sub memory space B and the sub memory space D correspondingly to the signal "0".

5 [0093]

In such a way, it is also possible to design the refresh control circuit 30 so as to intervene in the control of refreshment operation on more previous side (source side) in comparison with the first embodiment

10 from the point of view of the selection of row addresses at the time of refreshment.

[0094]

Incidentally, it is needless to say that the refresh control circuit 30 may be provided in the refresh address

15 counter 6.

[0095]

Moreover, it is also needless to say that, at the time of an ordinary operation, the intervening of the refresh control circuit 30 against the refresh address

20 counter 6 is stopped similarly to the first embodiment.

[0096]

[Third Embodiment]

[0097]

FIG. 8 shows the schematic configuration of a memory

25 device (DRAM) of a third embodiment. Incidentally, the same reference numerals as those in the first embodiment are attached to the similar components as those in the first embodiment, and they will be referred to as the same names as those in the first embodiment. Furthermore,

30 their detailed descriptions are omitted for simplifying the descriptions.

[0098]

  In the third embodiment, a refresh control circuit 30 is provided between a multiplexer 9 and a row decoder 10, or between a refresh address counter 6 and the multiplexer 9. The refresh control circuit 30 intervenes in the data (binary number code) which is not yet decoded and is input from the refresh address counter 6 to the row decoder 10 through the multiplexer 9 for specifying an address at the time of refreshment at the previous stage of the decoding (namely, at the previous stage before being input into the row decoder 10) so as not to perform the refreshment of the sub memory spaces which are not used.

[0099]

  For example, if a case where the sub memory space B is set to include the rows from the 32nd row (word line) to the 64th row and refreshment is omitted because the memory cells of each row in the sub memory space B have not been used until the refreshment is exemplified, the refresh control circuit 30 intervenes in the output of the multiplexer 9 or the output of the refresh address counter 6 so as not to output the codes from the binary number code = 0100000 corresponding to the 32nd row to the binary number code = 1000000 corresponding to the 64th row (for example, the binary number code = 0101000) to the row decoder 10.

[0100]

  Incidentally, it is needless to say that, at the time of an ordinary operation, the intervening of the refresh control circuit 30 against the refresh address counter 6 or the multiplexer 9 is stopped similarly to

the first embodiment.

[0101]

    As specifically shown in connection with the first embodiment, the second embodiment and the third embodiment, the configuration in which the refresh control circuit 30 according to an embodiment of the present invention is incorporated in a generally configured DRAM can omit refreshment to the memory spaces which are not in use at the time of the refreshment and does not need to be refreshed, and thereby can achieve the decrease of power consumption at least for the omission of the refreshment. Furthermore, it is possible to add the refresh control circuit 30 for performing such refresh control to the inside of a memory device having a general configuration such as a DRAM without causing the complication of the whole circuit configuration of the memory device.

[0102]

    Incidentally, it is needless to say that the concrete aspects of omitting refreshment to memory spaces which have not been used until the refreshment and is not necessary to be refreshed are not limited only to those of the first embodiment, the second embodiment and the third embodiment. Although each of the embodiments controls the selection of rows (row lines, or word lines) to omit the refreshment to the memory spaces unnecessary to be refreshed, the selection of the rows at the time of refreshment may be performed so as to select the rows line sequentially similarly in the case of ordinary self refreshment, and the sense amplifier 12 may not amplify the rows in the sub memory spaces which are unnecessary

to be refreshed even if the rows are selected and once read out by the column decoder 13. In such a way, because the rows in the sub memory spaces unnecessary to be refreshed are also once read at the time of

5   refreshment, the electrical energy for that reading is consumed. However, because the read signals are not amplified by the sense amplifier 12 (their amplification is omitted), at least the power consumption to be consumed at the amplification conventionally can be

10 decreased. It is needless to say that various other aspects can be adopted.